

CLAIMS

1. A semiconductor device comprising:
active areas where transistors are formed; and
5 a field area for isolating said active areas
from each other, said field area having a plurality of dummy
areas where dummy gates are formed.

2. The device as set forth in claim 1, wherein each of
said dummy areas is partitioned by a shallow trench isolation
10 layer.

3. The device as set forth in claim 1, wherein each of
said dummy gates has a reduced pattern of a respective one of
said dummy areas.

4. The device as set forth in claim 1, wherein said
dummy areas and said dummy gates are square.

5. The device as set forth in claim 1, wherein said
dummy areas and said dummy gates are rectangular.

6. The device as set forth in claim 1, wherein said
dummy areas and said dummy gates are polygonal.

7. The device as set forth in claim 1, wherein said
dummy areas and said dummy gates are circular.

8. The device as set forth in claim 1, wherein said
dummy areas are arranged in rows and columns.

9. The device as set forth in claim 8, wherein the rows
25 of said dummy areas are shifted from each other.

10. The device as set forth in claim 8, wherein the
columns of said dummy areas are shifted from each other.

11. The device as set forth in claim 8, wherein the rows
and columns of said dummy areas are shifted from each other.

12. A method for manufacturing a semiconductor device,
30 comprising the steps of:

forming a shallow trench isolation layer in a
semiconductor substrate, so that active areas and a field area
including dummy areas for isolating said active areas are
35 partitioned; and

forming gates on said active areas and dummy
gates on said dummy areas.

13. The method as set forth in claim 12, wherein said shallow trench isolation layer forming step comprises the steps of:

5 forming a first photoresist pattern layer using a first photomask having active area patterns corresponding to said active areas and dummy area patterns corresponding to said dummy areas;

10 forming a trench in said semiconductor substrate by a photolithography and etching process using said first photomask;

burying an insulating layer in said trench; and

performing a chemical mechanical polishing process upon said insulating layer.

15 14. The method as set forth in claim 13, wherein said gates and dummy gates forming step comprises the steps of:

forming a conductive layer over said semiconductor substrate;

20 forming a second photoresist pattern layer on said conductive layer, said second photoresist pattern layer having a gate pattern corresponding to said active areas and a dummy gate pattern corresponding to said dummy gates; and

25 patterning said conductive layer by a photolithography and etching process using said second photomask.

15. The method as set forth in claim 14, wherein said dummy gate pattern is constructed by a reduction of said dummy area patterns.

30 16. The method as set forth in claim 12, wherein said dummy areas and said dummy gates are square.

17. The method as set forth in claim 12, wherein said dummy areas and said dummy gates are rectangular.

35 18. The method as set forth in claim 12, wherein said dummy areas and said dummy gates are polygonal.

19. The method as set forth in claim 12, wherein said dummy areas and said dummy gates are circular.

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20. The method as set forth in claim 12, wherein said dummy areas are arranged in rows and columns.

21. The method as set forth in claim 20, wherein the rows of said dummy areas are shifted from each other.

5 22. The method as set forth in claim 20, wherein the columns of said dummy areas are shifted from each other.

23. The method as set forth in claim 20, wherein the rows and columns of said dummy areas are shifted from each other.

10 24. A photomask comprising:
a gate pattern for forming gates of transistors on a semiconductor substrate; and
dummy gate patterns, surrounding said gate patterns, for forming dummy gates on said semiconductor substrate,

15 said dummy gate patterns being constructed by a reduction of dummy area patterns for forming a shallow trench isolation layer in said semiconductor substrate.

25. The photomask as set forth in claim 24, wherein said dummy gate patterns are square.

20 26. The photomask as set forth in claim 24, wherein said dummy gate patterns are rectangular.

27. The photomask as set forth in claim 24, wherein said dummy gate patterns are polygonal.

25 28. The photomask as set forth in claim 24, wherein said dummy gate patterns are circular.

29. The photomask as set forth in claim 24, wherein said dummy gate patterns are arranged in rows and columns.

30. The photomask as set forth in claim 29, wherein the rows of said dummy gate patterns are shifted from each other.

30 31. The photomask as set forth in claim 29, wherein the columns of said dummy gate patterns are shifted from each other.

35 32. The photomask as set forth in claim 29, wherein the rows and columns of said dummy gate patterns are shifted from each other.

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